Morning

LASCAS: Thursday, March 2nd, 09:00 AM - 10:00 AM		
Session Tittle	**KEYNOTE 3**	
Title	Improving Integrity of Analog Layout Synthesis through Learning and Migration	
Speaker	Mark Po-Hung Lin	
Affiliation	National Yang Ming Chiao Tung University, Taiwan	

LASCAS: Thursday, March 2nd, 10:30 AM - 12:30 AM (7 papers)		
Session Tittle		**Special Session**
Track	**Paper #**	**Paper Title**
-	6800	Exploring Multi-Parameter Optimization of Automated HLS Tools and the Difficulty of Setting Complex Constraints
-	549	Security Implications of Decoupling Capacitors on Leakage Reduction in Hardware Masking
-	310	STT-MRAM Technology For Energy-Efficient Cryogenic Memory Applications
-	2326	Assessment of Dual Mode Logic for Approximate Computing
-	8343	Design Challenges of the CMOS Control Electronics Operating at Cryogenic Temperatures for Quantum Computing
-	8348	Overview of Cryogenic Operation in Nanoscale Technology Nodes
-	5834	Control Electronics for Scalable Spin-Based Quantum Computers

Circuit-to-system level optimization techniques toward enhanced energy-performance optimization and secured high speed VLSI for digital subsystems

Cryogenic Electronics: A Tool for Quantum Applications

Afternoon

LASCAS: Thursday, March 2nd, 02:00 PM - 03:00 PM		
Session Tittle	**KEYNOTE 4**	
Title	Classical Cryo-CMOS Systems for Quantum Computing: from a Wild Idea to Working Silicon	
Speaker	Edoardo Charbon	
Affiliation	École polytechnique fédérale de Lausanne (EPFL), Switzerland	

IBERCHIP: Thursday, March 2nd, 03:00 PM - 03:30 PM (4 papers)		
Session Title		**IBERCHIP**

LASCAS: Thurday, March 2nd, 03:30 PM - 05:30 PM (18 papers)		
Session Title		**Communication Circuits and Systems / Design Automation**
Track	**Paper #**	**Paper Title**
SC3	7369	Stacked-Cascode Current Steering Architecture for Gallium Nitride Variable-Gain LNAs
SC3	636	Active inductors modelling and trade-offs reexamined
SC3	7506	Minimizing Power Consumption Through Brute Force Algorithm in Elastic Optical Network
SC3	7060	Deep Learning-Based Receiver Energy Prediction in Energy Harvesting Wireless Sensor Network
SC4	2065	DNAr-analog: a library with a multiplexer to easily design, program, and simulate DSD analog circuits
SC4	2142	Quantitative Information Flow for Hardware: Advancing the Attack Landscape
Session Title		**Nano-Electronic Circuits and Systems / Energy-Efficient Circuits**
Track	**Paper #**	**Paper Title**
SC10	805	XNOR-Bitcount Operation using Computing-in-Memory with STT-MRAMs
SC10	3240	Performance Benchmarking of FinFET- and TFET-Based STT-MRAM Bitcells Operating at Ultra-Low Voltages
SC10	3373	Efficiency of Double-barrier Magnetic Tunnel Junction-based Digital eNVM array for Neuro-inspired Computing
SC1	6275	An Energy-Efficient StEFCal VLSI Design with Approximate Squarer and Divider Units
SC1	3001	A Fast Cold-Start Integrated System for Ultra-Low Voltage SC Energy-Harvesting Circuits
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Session Tittle		**Signal Image and Video Processing**
Track	**Paper #**	**Paper Title**
SC2	2860	Efficient Architecture for VVC Angular Intra Prediction based on a Hardware-Friendly Heuristic
SC8	9117	Complexity and Coding Efficiency Assessment of AOMedia Video 1
SC8	3626	Error Resilience Evaluation of Approximate Storage in the Motion Compensation of VVC Decoders
SC8	3646	Multi-Size Inverse DCT-II Hardware Design for the VVC Decoder
SC2	3791	High-Throughput and Multiplierless Hardware Design for the AV1 Fractional Motion Estimation
SC2	3183	Hardware Design for the Affine Motion Compensation of the VVC Standard