Tutorial Title: SPICE Transient Noise Simulations of Modern Integrated Circuits

Organizer and Speaker: **Léopold Van Brandt**

Noise simulations are traditionally performed in the frequency domain. This method is very suitable and efficient for analog circuits operating in small-signal conditions, around a fixed DC point, exemplified by amplifiers and filters. However, for circuits operating in large-signal conditions and/or exhibiting substantial nonlinearities, the effect of the noise must be analysed in the time domain. Important examples are digital logic gates as well as anaog switched-capacitor circuits, mixers and oscillators.

Industrial SPICE simulators such as Eldo® from Siemens EDA® or Virtuoso® Spectre® from Cadence® offer a transient noise analysis tool. Simulating the noise in the time domain requires to: (i) add individual physical noise sources in parallel with each noisy device (e.g. resistors, MOS transistors,…); (ii) generate independent random values at each time step; (iii) perform conventional transient simulations where the noise is handled as any other electrical signal. This framework results in a high computation time, which further increases when the statistical accuracy requires to perform many trials, and even more when the noise analysis is combined with process variations analysis.

While insightful and accurate as emulating real-world large-signal conditions for arbitrary nonlinear circuits, transient noise simulations turn out to be rarely encountered in the literature. The first reason is, undoubtedly, the high computation time mentioned above, difficult to fit in a design schedule; the second is, possibly, a lack of understanding of the specific simulation parameters. These points will be thoroughly addressed in this tutorial. We will describe and illustrate a robust and general simulation methodology, compatible with industrial tools, with case studies drawn from our recent research activities: ultra low-voltage SRAM bitcells that are prone to noise-induced bit flip when affected by several process variations; analog spiking neurons whose timing characteristics are degraded by the combined effects of process variability and intrinsic noise. Finally, the generation of physics-based random telegraph noise and its incorporation in SPICE simulations will be explained in the tutorial.

Biography

Léopold Van Brandt was born in Belgium, in 1995. He received the B.S. and the M.S. degrees in Electrical Engineering from the Université catholique de Louvain, Louvain-la Neuve, in 2015 and 2017, respectively, and the PhD degree in Engineering Science for his dissertation entitled “Statistical Analyses of Intrinsic Noise and Variability Effects in CMOS Digital Latches” in 2022. He then worked for two years as a postdoctoral research fellow in the Mathematical Engineering department of the UCLouvain on the project “Thermodynamics of Circuits for Computation”. Since October 2024, he has been leading his own postdoctoral research project entitled “Stochastic Modelling of Present and Future Nonlinear Dynamical Electronic Devices and Circuits”.

His research interests include but are not limited to: nanoelectronics; characterisation and modelling of the noise in nonlinear devices and circuits; circuit simulation theory; circuit reliability assessment (notably CMOS SRAM bitcells); stochastic thermodynamics; analog neuromorphic circuits and sensors, memristive and ferroelectric devices.

The interplay between research and education is one of his major concerns.

Non-exhaustive list of publications directly related to the tutorial:

Van Brandt, L., Bonnin, M., da Silva, M. B., Bolcato, P., Wirth, G. I., Flandre, D., & Delvenne, J. C. (2025). Modeling and Predicting Noise-Induced Failure Rates in Ultra Low-Voltage SRAM Bitcells Affected by Process Variations. *IEEE Transactions on Circuits and Systems I: Regular Papers*. *Special Issue of LASCAS 2024*.
https://ieeexplore.ieee.org/abstract/document/10836927
https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=10506179

Van Brandt, L., Silveira, F., Delvenne, J. C., & Flandre, D. (2023). On noise-induced transient bit flips in subthreshold SRAM. *Solid-State Electronics*, *208*, 108715.
https://www.sciencedirect.com/science/article/pii/S0038110123001284

Wirth, G. I., Both, T.H., da Silva, M. B., & Van Brandt, L. (2025). Statistical Modeling of Timing Variability due to Random Telegraph Noise in Logic Gates. *Fluctuation and Noise Letters*, in press.